REMARKS

This amendment is responsive to the Office Action dated December 21, 2001. No fee is believed due, but if there is a fee deficiency, please charge Deposit Account No. 06-1050.

Claims 1-12 have been examined. Claims 13-21 have been withdrawn from consideration. Claims 4 and 10 have been amended. Claims 22-27 have been added. Support for the amendments and the new claims can be found in the specification, drawings and the claims. No new matter has been added. Claims 1-3, 5-9, and 11-12 have been cancelled. Claims 4, 10, and 22-27 are pending.

The substitute specification has been amended in accordance with objections stated in the Office Action. In addition, the substitute specification has been amended in view of the amendments to the drawings explained below. No new matter has been added.

In view of the above amendments and the following remarks, the applicants respectfully request withdrawal of each of the rejections and allowance of the application. Applicant's remarks, below, are preceded by quotations of the related comments of the Examiner, in small, bold-face type.

Drawings

It should be noted that any changes to the drawing sheets have been marked in red to show the changes.

> **2. Figure 12 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.**

Enclosed is a substitute drawing sheet labeled FIG. 12 that includes the designation -- Prior Art--.

3. The drawings are bjected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "70" and "71" have been used to designate both chip and bridge. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Enclosed is a new drawing sheet labeled FIG. 6 that has been amended. Specifically, the reference characters "70", "71" in FIG. 6 refer to a bridge "53A", "53B" as shown in FIG. 5 and as described on page 13, lines 13-15 of the specification. So the reference character "70" has been replaced with "53A" and the reference character "71" has been replaced with reference character "53B" to conform the drawings with the specification.

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "4" and '12" have both been used to designate first die pad. A proposed drawing correction or corrected drawings are required in reply to the office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Enclosed is a new drawing sheet labeled FIG. 12 that has been amended. In particular, since the reference character "12" refers to the "coupling piece" as shown in FIG. 12, the arrow associated with the reference character has been modified to more clearly point to the coupling piece. Support for this amendment can be found, for example, on page 2, lines 16-18 of the application.

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: reference characters "56C" in Fig. 3A, "59A" in Fig. 4A, "59B"in Fig. 4A, "60A" in Fig. 4A and "11" in Fig. 12 are not referenced in the specification of instant invention. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Enclosed are new drawing sheets labeled FIG. 3A, 4A, and 12 that have been amended. These reference characters have been removed from the figures.

6. The drawings are objected to because reference numbers '81" in Fig. 7 and "80" in Fig. 11 are not pointing correct structure in the figures. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The object to the drawings will not be held in abeyance.

7. The drawings are bjected to as failing t comply with 37 CFR 1.84(p)(5) because they d n t include the foll wing reference sign(s) mentioned in the description: the reference character "O" in the specification is not referenced in the figures. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Enclosed are new drawing sheets labeled FIG. 7 and 11 that have been amended. Specifically, the arrow associated with reference character "81" has been corrected to more clearly point to the plate in FIG. 7. (see page 13, line 33 of the application) In addition, the arrow associated with the reference character "80" has been corrected to more clearly point to the semiconductor device in FIG. 11. (see page 13, lines 21-22 of the application)

8. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the first and second semiconductor chip which are superposed on each other, at least one bridge arranged between said first and second semiconductor chip, and the insulating resin exposes the rear surface of each of said bridge must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Enclosed are new drawing sheets labeled FIGS. 1A, 2A, 3A, and 4A that have been amended. A new reference character "92" designates the feature associated with the reference character "O". Support for such an amendment can be found, for example, on page 8, lines 7-8 of the application. The specification has been amended to conform the drawings to the specification.

The subject matter recited in claim 10 has been clarified by replacing the limitation "arranged between" with "at least one bridge electrically connecting said first and said second semiconductor chip." In addition, the limitation "superposed" recited in claim 10 has been replaced with "formed" so as to clarify the subject matter.

9. Applicant is required to submit a proposed drawing correction to this Office action. However, formal correction of the noted defect may be deferred until after the examiner has considered the proposed drawing correction. Failure to timely submit the proposed drawing correction will result in the abandonment of the application.

In view of the above corrections and remarks, applicants respectfully request withdrawal of the objections to the drawings.

Specification

10. The disclosure is objected to because of the following informalities:

Abstract, line 3, erase some extra spaces before "they."

The specification needs an extra line before sub-titles.

On pages 2 and 15, removes "..."

On page 2, line 15, needs a space before 7.

On page 6, lines 26 and 28, "the bonding pad" should be --a bonding pad--.

On page 11, line 12, removes some extra space between "the" and "external."

On page 13, line 12, removes some extra space between "the" and "semiconductor."

On page 19, line 7, removes some extra space before "a."

The specification does not have a brief description of the Figs. 1A - 1E, Figs. 2A - 2E, Figs. 3A - 3E, and Figs. 4A - 4E. Also, the brief descriptions of each figure are not clearly describing the drawings and contain some errors such as Fig. 1 -6 are a view of a "first" semiconductor device.

Enclosed is a substitute specification that has been corrected to overcome the informalities objected to in the disclosure. No new matter has been added.

In view of the above corrections, applicants respectfully request withdrawal of the objections to the specification.

Claim Rejections – 35 U.S.C. § 112

11. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. Claims 10 - 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the inventi n.

In claim 10, it can n t be determined what the applicant regards as the "first and sec nd semiconduct r chip which are superposed n each ther, at least one bridge arranged

between said first and sec nd semiconductor chip, and the insulating resin exposes the rear surface of each of said bridge". Further, the arrangement f the bridge in the claimed structure is not clear. Therefore the arrangement of the bridge in the claimed structure must be clearly defined in the specification or the claim cancelled from instant invention. No new matter should be entered.

Claim 10 has been amended to clarify the subject matter as explained above in section 9 of the Office Action. Claims 11-12 have been canceled.

The applicants respectfully assert that claim 10 is no longer indefinite and request withdrawal of the 35 U.S.C. § 112 rejection.

Claim Rejections – 35 U.S.C. § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. Claims 1 - 6 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Ugon.

Note Figs. 6 and 7 of Ugon, where he/she shows a semiconductor device comprising: a first (43) and a second (44) semiconductor chip which are electrically connected to each other (see Fig. 6); a bridge (47b) arranged between said first and said second semiconductor chip and electrically connecting them (see Fig. 6); external connecting electrodes (48a and 48c) provided to surround areas where said first and said second semiconductor chip are located, at least a portion of the rear surface of them serving as an electrode to be externally connected (see Figs. 6 and 7); first metallic wires (46) which electrically connect said first and said second semiconductor chip to said external connecting electrodes, respectively (see Figs. 6 and 7); second metallic wires (46 in middle) which electrically connect said first and said second semiconductor chip to said bridge (see Figs. 6 and 7); and insulating resin (49) which seals said first and second semiconductor chip, said external connecting electrodes, and said first and said second metallic wires (see Fig. 7), wherein said insulating resin (49) exposes the rear surface of each of said bridge and said external connecting electrodes (see Fig. 7), and said second metallic wires are ball-bonded on said first and said second semiconductor chip and stitch-bonded on said bridge. Further, since Ugon does not limit the sealing material to any particular or specific sealing material, his/her disclosure encompasses all well known sealing material including "resin." Even further, the phrase "said second metallic wires are ball-bonded on said first and said second semiconductor chip and stitch-bonded on said bridge" is a method of forming a device, which is not germane to the issue of patentability of the device itself. Therefore, this limitation has not been given patentable weight.

Regarding claims 2 and 5, Ugon discloses the rear surface of each of said insulating resin and said badge is coated with an insulating film (42 in Fig. 7 and column 7, liens 35 - 37).

Regarding claims 3 and 6, note Fig. 7 of Ugon, where he/she shows the rear surface of each of said insulating resin, said bridge and said external connecting electrodes is coated with an insulting film (42 in Fig. 7 and column 7, lines 35 - 37) so that said external connecting electrodes are partially exposed (see Fig. 7).

Regarding claim 4, note Fig. 7 of Ugon, where he/she shows a semiconductor device comprising: a first (43) and a second (44) semiconductor chip which are electrically connected to each other (see Figs. 6 and 7); a first die pad (47a, the left) to which said first semiconductor chip is fixed (see Figs. 6 and 7); a second die pad (47a, the right) to which said second semiconductor chip is fixed (see Figs. 6 and 7); at least one bridge (47b) arranged between said first and said second semiconductor chip and electrically connecting them (see Figs. 6 an d7); external connecting electrodes (48a and 48c) provided to surround areas where said first and said second semiconductor chip are located, at least a portion of the rear surface of them serving as an electrode to be externally connected (see Figs. 6 and 7); first metallic wires (46) which electrically connect said first and said second semiconductor chip to said external connecting electrodes, respectively (see Figs. 6 an d7); second metallic wires (46 in middle) which electrically connect said first semiconductor chip, said bridge and said second semiconductor chip (see Figs. 6 and 7); and insulating resin (49) which seals said first and said second semiconductor chip, said external connecting electrode, and said first and said second metallic wires (see Fig. 7), wherein said insulating resin (49) exposes the rear surface of each of said bridge and said external connecting electrodes (see Fig. 7), and said second metallic wires are ball-bonded on said first and said second semiconductor chip and stitch-bonded on said bridge. Further, since Ugon does not limit the sealing material to any particular or specific sealing material, his/her disclosure encompasses all well known sealing material including "resin." Even further the phrase "said second metallic wires are ball-bonded on said first and said second semiconductor chip and stitch-bonded on said bridge" is a method of forming a device, which is not germane to the issue of patentability of the device itself. Therefore, this limitation has not been given patentable weight.

Regarding claim 12, note Fig. 7 of Ugon, where he/she shows the rear surface of each of said insulating resin, said first and said second die pad, said bridge and said external connecting electrodes is coated with an insulating film (42 in Fig. 7 and column 7, lines 35 - 37) so that said first die pad, said second die pad and/or said external connecting electrodes are partially exposed (see Fig. 7).

Claim 4 has been amended to recite a device that includes a first and second die and external connecting electrodes, further comprising

-- further comprising a plurality of recesses in a rear surface of said insulating resin, the rear surface of said first and second die pad and said external connecting electrodes are exposed within said recesses--.

As shown in FIG. 1D, the device includes die pads and the external connecting electrodes 52 that are formed to have a rear surface portion that has recesses 63. (see page 8, lines 10-12 of the application) By adjusting the depth of the recesses 63, the amount of brazing material and

conductive paste formed can be controlled to adjust the bonding strength. (see page 8, lines 12-14 of the application)

Ugon discloses a flat package that includes two devices 43, 44 and a linking conductor 46 connected between a conductor 47 and the two devices. (see FIG. 7). Each of the two devices 43, 44 include a rear surface in contact with a wafer 42 having a flat surface and does **not** disclose "a plurality of recesses in a rear surface of said insulating resin, the rear surface of said first and second die pad and said external connecting electrodes are exposed within said recesses" as recited in claim 4 of the present invention. Ugon does not disclose a semiconductor device having the features quoted above. Thus, Ugon does not disclose, teach or suggest a semiconductor device as recited in claim 4 and is patentably distinct thereover.

Moreover, claim 4, as amended, recites a device that includes second metallic wires such that the "second metallic wires are coupled to said first and said second semiconductor chip using a ball-bond and coupled to said bridge using a stitch-bond."

Although Ugon discusses the use of an output pad 45 to connect the linking conductor 46 to conductor 47, it makes no mention of a "stitch bond" or "ball bond" type bond as claimed in the present invention. (see column 5, lines 60-64 and FIGS. 6-7) Ugon does not disclose a semiconductor device having the features quoted above. Thus, Ugon does not disclose, teach or suggest a semiconductor device as recited in claim 4 and is patentably distinct thereover.

Consequently, the applicants respectfully request withdrawal of the 35 U.S.C. § 102(b) rejection of claim 4. Claims 1-3 and 5-6 have been canceled.

15. Claims 1 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Lin et al.

Regarding claims 1 and 4, note Fig. 3 of Lin et al., where he/she shows a semiconductor device comprising: a first (17) and a second (15) semiconductor chip which are electrically connected to each other (see Fig. 3); a second die pad (19, the right) to which said second semiconductor chip is fixed (see Fig. 3); at least one bridge (13, the middle) arranged between said first and said second semiconductor chip and electrically connecting them (see Fig. 3); external connecting electrodes (13) provided to surround areas where said first and said second semiconductor chip are located, at least a portion of the rear surface of them serving as an electrode to be externally connected (see Fig. 3); a first metallic wires (18) which electrically connect said first and said second semiconductor chip to said external c nnecting electr des, respectively (see Fig. 3); sec nd metallic wires (18 in middle) which electrically c nnect said first semic nductor chip, said bridge and said second semic nduct r chip (see Fig. 30; and insulating resin (20) which seals said first and said sec nd semiconduct r chip, said external connecting electrode, and said first and said sec nd

metallic wires (see Fig. 13), wherein said insulating resin (20) exposes the rear surface of each of said bridge and said external c nnecting electrodes (see Fig. 3), and said second metallic wires are ball-bonded on said first and said second semiconductor chip and stitch-bonded on said bridge. Further, the phrase "said second metallic wires are ball-bonded on said first and said second semiconductor chip and stitch-bonded on said bridge" is a method of forming a device, which is not germane to the issue of patentability of the device itself. Therefore, this limitation has not been given patentable weight.

Lin et al. discloses a method of fabricating a semiconductor device that includes first and second semiconductor devices 15, 17, a conductive trace 13, and a bond wire 18 connected between the trace 13 and the first and second semiconductor devices. (see FIG. 3) However, the rear surfaces of these elements do **not** disclose "a plurality of recesses in a rear surface of said insulating resin, the rear surface of said first and second die pad and said external connecting electrodes are exposed within said recesses" as recited in claim 4 of the present invention. Thus, Lin et al. does not teach or suggest a semiconductor device as recited in claim 4 and is patentably distinct thereover.

Moreover, although Lin et al. discloses several methods of forming a connection between these components, it makes no mention of a "stitch bond" or "ball bond" type bond as used in the present invention. (see column 3, lines 35-39 and FIG. 3) Lin et al. does not disclose a semiconductor device having the features quoted above as recited in claim 4. Thus, Lin et al. does not teach or suggest a semiconductor device as recited in claim 4 and is patentably distinct thereover.

Consequently, the applicants respectfully request withdrawal of the 35 U.S.C. § 102(b) rejection of claim 4. Claim 1 has been canceled.

16. Claims 7 - 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Fukui et al.

Note Figs. 7(a) and 1 of Fukui et al., where he/she shows a semiconductor device comprising: a first (1) and a second (2) semiconductor chip which are superposed on each other (see Fig. 7(a)); a bridge (4, the left) electrically connecting said first and said second semiconductor chip (see Fig. 7(a)); external connecting electrodes (4) provided to surround areas where said first and said second semiconductor chip are located, at least a portion of the rear surface of them serving as an electrode to be externally connected (see Figs. 7(a) and 2(g)); first metallic wires (8) which electrically connect said first and said second semiconduct r chip to said external connecting electr des, respectively (see Fig. 7(a)); second metallic wires (8 on top f 4, the left) which electrically c nnect said first and said second semic nductor chip t said bridge (see Fig. 7(a)); and insulating resin (9) which seals said first and said second semic nductor chip, said external connecting electrode, and said first

and said second metallic wires (see Fig. 1), wherein said insulating resin (9) expos s the rear surface of each of said bridge and said external connecting electrodes (see Fig. 1), and said second metallic wires re ball-bonded on said first and said second semiconductor chip and stitch bonded on said bridge. Further, the phrase "said second metallic wires are ball-bonded on said first and said second semiconductor chip and stitch-bonded on said bridge" is a method of forming a device, which is not germane to the issue of patentability of the device itself. Therefore, this limitation has not been given patentable weight.

Regarding claim 8, Fukiu et al. discloses the rear surface of each of said insulating resin and said bridge is coated with an insulating film (3 in Fig. 1).

Regarding claim 9, Fukiu et al. discloses the rear surface of each of said insulating resin, said bridge and said external connecting electrodes is coated with an insulating film (3 in Fig. 1), so that said external connecting electrodes are partially exposed (see Fig. 1).

Claims 7-9 have been canceled, consequently the applicants respectfully request withdrawal of the 35 U.S.C. § 102(b) rejection directed to these claims.

Claim Rejections – 35 U.S.C. § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goto in view of Fukase et al.

Goto discloses the claimed invention except for an insulating resin for sealing said first and said second semiconductor chip, said external connecting electrode, and said first and said second metallic wires, wherein said insulating resin exposes the rear surface of each of said bridge and said external connecting electrodes; and an insulating film for coating the rear surface of each of said insulating resin, said first die pad and said bridge. However, Fukase et al. discloses an insulating resin (24 in Fig. 1(e)) for sealing said first and said second semiconductor chip, said external connecting electrode, and said first and said second metallic wires, wherein said insulating resin exposes the rear surface of each of said bridge and said external connecting electrodes (see Fig. 1(e)); and an insulating film (10 in Fig. 1(e)) for coating the rear surface of each of said insulating resin, said first die pad and said bridge (see Fig. 1(e)). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Goto by including the insulating resin and the insulating film as taught by Fukase et al. The ordinary artisan w uld have been motivated to m dify G to in the manner described ab ve f r at least the purp se of increasing reliability f the package. Further, the phase "said second metallic wires are ball-bonded n said first and said sec nd semic nductor chip and stitch-bonded on said bridge" is a method

f f rming a device, which is not germane to the issue of patentability f the device itself. Theref re, this limitation has not been given patentable weight.

Regarding claim 11, Goto, as modified, discloses the rear surface of each of said insulating resin, said first die pad and said bridge is coated with an insulating film (3 in Fig. 1).

Goto discloses a semiconductor device having a chip 2 formed over chip 1 connected together by a thin metal wire 4. (see FIG. 1) As shown in FIG. 1(e) in Fukase et al., a semiconductor chip 16 is wire bonded to circuit patterns 12 using bonding wires 18. However, neither reference appears to disclose "a plurality of recesses in a rear surface of said insulating resin, the rear surface of said first and second die pad and said external connecting electrodes are exposed within said recesses" as recited in claim 10 of the present invention.

Moreover, neither reference appears to mention using a "stitch bond" or "ball bond" type bond as used in the present invention. Thus, neither reference teaches or suggests a semiconductor device as recited in claim 10 and is patentably distinct thereover.

Consequently, the applicants respectfully request withdrawal of the 35 U.S.C. § 103(a) rejection of claim 10. Claim 11 has been canceled.

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Huang et al., Nakamura, Spielberger et al., Weinberg et al., Tang et al., Han et al., Sasaki, Hobson, and Kweon et al. disclose a semiconductor device.

The prior art of record and not relied upon has not been discussed herein because those references have not been applied to any of the claims.

New Claims

New dependent claims 22-23 depend on independent claim 4. The new claims refer to features associated with the recess feature. Support for claim 22 can be found, for example, on page 6, lines of the application. Likewise, support for claim 23 can be found, for example, on page 6, lines of the application. No new matter has been added. As explained above, claim 4 is patentably distinct thereover. Consequently, claims 22-23 should be allowable for at least the same reasons as for claim 4.

Likewise, claims 24-25 are new dependent claims that depend on independent claim 10. The comments made to the claims above also apply to these claims. Consequently, claims 24-25 should be allowable for at least the same reasons as for claim 10.

New independent claims 26 and 27 have been added that includes a further limitation directed to the recess portion of the rear surface of the semiconductor device. Support for claims 26 and 27 can be found, for example, on page 8, lines 1-8 of the application and in the original claims. No new matter has been added. The applicant's submit that none of the cited references disclose, teach or suggest the limitations recited in claims 26 and 27, thus these claims should be allowable.

Attached is a marked-up version of the changes being made by the current amendment.

Applicant asks that all claims be allowed. Enclosed is a $276 check for excess claim fees. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: March 21, 2002

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Version with markings to show changes made

In the specification:

Please substitute the specification with the amended specification provided herein.

In the claims:

Claims 1-3, 5-9, and 11-12 have been cancelled.

Claims 4 and 10 have been amended.

4. (Amended) A semiconductor device comprising:

a first and a second semiconductor chip which are electrically connected to each other;

a first die pad to which said first semiconductor chip is fixed;

a second die pad to which said second semiconductor chip is fixed;

at least one bridge arranged between said first and said second semiconductor chip and electrically connecting them;

external connecting electrodes provided to surround areas where said first and said second semiconductor chip are located, at least a portion of the rear surface of them serving as an electrode to be externally connected;

first metallic wires which electrically connect said first and said second semiconductor chip to said external connecting electrodes, respectively;

second metallic wires which electrically connect said first semiconductor chip, said bridge and said second semiconductor chip; and

insulating resin which seals said first and said second semiconductor chip, said external connecting electrode, and said first and said second metallic wires,

wherein said insulating resin separates said first and second die pad, said bridge and said external connecting electrodes from one another [exposes the rear surface of each of said bridge and said external connecting electrodes], and said second metallic wires are [ball-

bonded on] coupled to said first and said second semiconductor chip using a ball bond and [stitch-bonded on] coupled to said bridge using a stitch bond,

further comprising a plurality of recesses in a rear surface of said insulating resin, the rear surface of said first and second die pad and said external connecting electrodes being exposed within said recesses.

10. (Amended) A semiconductor device comprising:

a first and a second semiconductor chip which are superposed on each other;

a first die pad to which said first semiconductor chip at a lower layer is fixed;

at least one bridge arranged between said first and said second semiconductor chip and electrically connecting them;

external connecting electrodes provided to surround areas where said first and said second semiconductor chip are located, at least a portion of the rear surface of them serving as an electrode to be externally connected;

first metallic wires which electrically connect said first and said second semiconductor chip to said external connecting electrodes, respectively;

second metallic wires which electrically connect said first semiconductor chip, said bridge and said second semiconductor chip; and

insulating resin which seals said first and said second semiconductor chip, said external connecting electrode, and said first and said second metallic wires,

wherein said insulating resin exposes the rear surface of each of said bridge and said external connecting electrodes, and said second metallic wires are [ball-bonded on] coupled to said first and said second semiconductor chip using a ball bond and [stitch-bonded on] coupled to said bridge using a stitch bond,

further comprising a plurality of recesses in a rear surface of said insulating resin, the rear surface of said first and second die pad and said external connecting electrodes being exposed within said recesses.

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SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a semiconductor device and a method of manufacturing it, and more particularly to a semiconductor device in which a plurality of semiconductor chips are mounted a planar or superposed manner and a method of manufacturing it.

2. Description of the Related Art

In recent years, in order to increase the capacity of a memory and also extend the circuit function, a plurality of chips are mounted in a single package.

For example, as shown in Fig. 12, a semiconductor device 3 with two semiconductor chips 1 and 2 arranged two-dimensionally is mounted in a single package. The semiconductor device 3 is formed in a lead frame in which a large number of leads 6 are arranged around a first die pad 4 and a second die pad 5. Bridges 7 are arranged between the first die pad 4 and the second die pad 5. The first semiconductor chip 1 is fixed onto the first die pad 4, whereas the second semiconductor chip 2 is fixed onto the second die pad 5. The first bonding pads 8 and 8a on the first and second chips 1 and 2 and the second bonding pads 9 on the leads 6 are connected to each other by metallic wires 10, respectively. The first semiconductor chip 1 and the second semiconductor chip 2 are electrically connected to each other by the bridges 7. The bonding pads 8 of the first semiconductor chip 1 and the bridges 7 are connected to each other by the metallic wires, respectively. Likewise the bridges 7 and the bonding pad 8a on the second semiconductor chip 2 are connected to each other by the metallic wires 10. The entire semiconductor

device is mounted in a single package by insulating resin.

Each metallic wire 10 is connected so that its one end is subjected to ball bonding whereas its other end is subjected to stitch bonding. Since the stitch bonding during which ultrasonic wave is applied for a long time deteriorates the semiconductor chip, the ball bonding is adopted on the side of the semiconductor chip, whereas the stitch bonding is adopted on the side of the bonding pad on the lead 6.

However, where the first semiconductor chip 1 and the second semiconductor chip 2 are directly connected to each other by the metallic wires 10, either one of them must be necessarily connected by the stitch bonding. In order to obviate such an inconvenience, in this configuration, the bridges 7 are used to connect both semiconductor chips by the ball bonding.

However, with respect to the lead frame as shown in Fig. 12, the leads 6, which are coupled via a tie bar, can be easily handled. However, the bridges 7, each of which is formed in an island shape, will drop when it stands now. In order to prevent this, various schemes are proposed.

Now, a coupling piece 12 is formed for coupling the first die pad 4 and second die pad 5 with each other. The coupling piece 12 and the bridges 7 are bonded to each other by an adhesive tape.

However, the adhesive tape 13, to which heat is applied during molding, is required to have heat resistance and hence expensive. This leads to cost up of the semiconductor device.

Another technique for supporting the bridges 7 so that they will not drop is to form a lead pattern inclusive of the bridges 7 on a supporting board such as a flexible sheet, a ceramic board and a printed board and mold it. However, adoption of the supporting board increases the thickness of the semiconductor device, and so leads to cost up thereof. Further, the semiconductor chip molded on the supporting board is thermally insulated by the supporting board. This leads to temperature rise of the semiconductor chip. The temperature rise of the semiconductor chip gives rise to reduction of the driving current and driving frequency. This makes it impossible to bring out the inherent capability of the semiconductor chip.

SUMMARY OF THE INVENTION

This invention has been accomplished in view of the problem described above. Firstly, this invention solves the problems by a semiconductor device comprising:

a first and a second semiconductor chip which are electrically connected to each other;

a bridge arranged between the first and the second semiconductor chip and electrically connecting them;

external connecting electrodes provided to surround areas where the first and the second semiconductor chip are located, at least a portion of the rear surface of them serving as an electrode to be externally connected;

first metallic wires which electrically connect the first and the second semiconductor chip to the external connecting electrodes, respectively;

second metallic wires which electrically connect the first and the second semiconductor chip to the bridge; and

insulating resin which seals the first and the second semiconductor chip, the external connecting electrode, and the first and the second metallic wires,

wherein the insulating resin exposes the rear surface of each of the bridge and the external connecting electrodes, and the second metallic wires are ball-bonded on the first and the second semiconductor chip and stitch-bonded on the bridge.

As understood from the method of manufacturing a semiconductor as described later, since the bridge and external connecting electrodes are supported by the insulating resin, unlike the prior art, no adhesive tape is required. In addition, since the rear surface of the semiconductor chip is directly mounted a mounting board, a temperature rise in the semiconductor chip can be prevented.

Secondly, since the rear surface of each of the insulating resin and the bridge is coated with an insulating film, the wirings on the mounting board can be extended to the rear surface of the bridge, thereby simplifying the wiring pattern on the side of the

mounting board.

Thirdly, since each of the insulating resin, the bridge and the external connecting electrodes is coated with an insulating film, and the external connecting electrodes are partially exposed, these connecting electrodes can be connected to the electrodes of the side of the mounting board.

Fourthly, this invention solves the above problem by a method of manufacturing a semiconductor device comprising the steps of:

preparing a sheet-like plate having a prescribed thickness, the plate having a flat rear surface over an entire region corresponding to a resin sealing area and a front surface in which external connecting electrodes and a bridge are formed as convex shapes in a region encircled by a region in contact with an upper mold;

mounting a semiconductor chip on an area where it is to be mounted and electrically connecting the semiconductor chip to the external electrodes and the bridge, respectively;

mounting the plate in a mold and filling a space formed by the plate and the upper mold with insulating resin; and

removing the plate exposed to the rear surface of the insulating resin, thereby separating the convex portions.

Until the steps of mounting the semiconductor chips, electric connection and filling the insulating resin, the plate constituting connecting electrodes and bridge is used as a supporting board. Separation of the external connecting electrodes and bridge is performed using hardened insulating resin as a supporting board. Therefore, the supporting board such as a printed board, ceramic board which were conventionally adopted is not required. The bridge can also be made without using the adhesive tape.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A-E show a semiconductor device according to this invention.

Figs. 2A-E show a semiconductor device according to this invention.

Figs. 3A-E show a semiconductor device according to this invention.

Figs. 4A-E show a semiconductor device according to this invention.

Fig. 5 is a view showing a semiconductor device according to this invention.

Fig. 6 is a view showing a semiconductor device according to this invention.

Fig. 7 is a view showing the method of manufacturing a semiconductor device according to this invention.

Fig. 8 is a view showing the method of manufacturing a semiconductor device according to this invention.

Fig. 9 is a view showing the method of manufacturing a semiconductor device according to this invention.

Fig. 10 is a view showing the method of manufacturing a semiconductor device according to this invention.

Fig. 11 is a view showing the method of manufacturing a semiconductor device according to this invention.

Fig. 12 is a view showing the semiconductor device using a conventional lead frame.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiment 1 explaining the semiconductor device according to the invention.

Fig. 1A is a plan view of a semiconductor device according to the invention. Figs. 1B–1E are sectional views taken in line A–A in Fig. 1A. Figs. 1B–1E show four types of the rear-surface structure of the semiconductor device.

In this invention, a first die pad 50 and a second die pad 51 are arranged on substantially the same plane, and external connecting electrodes 52 are formed around them. The front surface of each of the connecting electrodes 52 serves as a bonding pad whereas the rear surface thereof is externally connected. At least one bridge 53 is formed between the first die pad 50 and the second die pad 51.

A first semiconductor chip 54 is fixed onto the first die pad 50, whereas a second

semiconductor chip 55 is fixed onto the second die pad 51. These semiconductor chips 54 and 55 are connected to each other by metallic wires.

The metallic wires include a first metallic wire 56 connected to the external connecting electrode 52 and a second metallic wire 57 connected to the bridge 53. A plurality of bonding pads are formed on the surface of each semiconductor chip. On the basis of input signal to the bonding pads, at least a part of the bonding pads are selected. The positions and number of the external connecting electrodes are correspondingly determined. The selected bonding pads 58 on the semiconductor chip and the external connecting electrodes 52 are connected to each other by means of the first metallic wires 56.

On the other hand, the first semiconductor chip 54 and the second semiconductor chip 55 are connected in such a manner that a bonding pad 59 of the former and the one end of the bridge 53 are connected to each other by the second metallic wire 57 and the other end of the bridge 53 and a bonding pad 60 of the second semiconductor chip 55 are connected to each other by the second metallic wire 57.

In this configuration described above in which the bridge 53 is provided, all the metallic wires 56, 57 on the side of each of the first and second semiconductor chips 54, 55 are made connectable by ball bonding.

As understood from the description of Figs. 7–11, the external connecting electrode 52 and bridge 53 are supported in such a manner that the conductive foil is half-etched and they are molded and supported by insulating resin 61 before they are completely separated.

The feature of this invention resides in that the external connecting electrodes 52 and the bridge 53 are not supported by a coupling piece such as a supporting lead and tab suspending lead, but are independently sealed by insulating resin 61. In addition, the feature resides in that these independent external connecting electrodes 52 and bridge(s) 53 are sealed without using the adhesive tape. Therefore, the completed product of the semiconductor device has no cutting portion of the above coupling piece.

A conventional lead frame has been completed by cutting the coupling member such as a suspending lead and a tie bar. Namely, the lead is machined as a completed product from the front surface to the side and rear surfaces thereof. The lead from which

is a completed product requires a coupling member. After the semiconductor chip is mounted on the lead frame, it is sealed by insulating resin, and the coupling member is cut. Therefore, the bridge 7 arranged in the form of an island without being connected to anywhere must be fixed by the supporting member such as the adhesive tape as shown in Fig. 12.

On the other hand, in accordance with this invention, on the side of a lead frame manufacturer, the conductive foil is half-etched, and the external connecting electrodes 52 and bridge(s) 53 are supplied, in a semi-completed state, to a semiconductor manufacturer. On the side of the semiconductor manufacturer, the semiconductor device is subjected to the packaging, electric connection and sealing by insulating resin. Finally, the rear surface of the external connecting electrode 52 and bridge(s) 53 is machined. Therefore, the semiconductor device can be completed without adopting the coupling member such as the tab suspending lead and adhesive tape, and with no mechanical separation of the coupling member.

The rear surface of the insulating resin 61 is exposed in its shaded areas in Fig. 1A. This state is shown in Fig. 1B. The semiconductor device is secured on a mounting board at the electrodes formed on the mounting board to correspond to the above exposed areas. In this case, the heat generated from the semiconductor chips 54, 55 radiated toward the electrodes on the mounting board through the die pads 50, 51 having excellent thermal conductivity. The conventional semiconductor, in which the entire area is packaged or only the solder ball is made of a thermally conductive member in SMD, exhibits poor heat radiating characteristic, and hence could not show the greatest capability of the semiconductor chip. In contrast, the semiconductor device according to this embodiment exhibits excellent heat radiating characteristic and can show the great capability of the semiconductor chip.

Fig. 1C shows a first modification of the above structure (Fig. 1B). In Fig. 1B, in which the shaded areas are exposed, it was difficult to extend the wirings on the mounting board to the rear surface of the semiconductor device. Further, when a brazing material is applied to the external connecting electrode 52 and die pads 50, 51, the thickness of the solder differs because of a difference in the areas so that the semiconductor device tilted.

This invention intends to solve the above problem by forming an insulating film 62 on the rear surface of the semiconductor device as shown in Fig. 1C. The dotted circles 92 shown in Fig. 1A show the external connecting electrodes 52, and die pads 50 and 51 exposed from the insulating film 62. In other words, since the other areas than the circle O marks 92 are covered with the insulating film 62, the wirings formed on the mounting board can be extended to the rear surface of the semiconductor device.

Since the areas of the O marks 92 are approximately equal to one another, the thickness of the brazing material does not substantially differ. This applies after solder printing or reflow, and also applies to the conductive paste such as Ag, Au, Ag-Pd.

A second modification is shown in Fig. 1D. As seen from Fig. 1D, the rear surface of each of the die pads 50, 51 and the external connecting electrodes 52 is formed to be concave from that of the insulating resin 61. By adjusting the depth of these concave portions 63, the amount of the brazing material and conductive paste formed there can be controlled to adjust the bonding strength. Further, because of the presence of the convex portions 64 of the insulating resin 61, the solder or conductive paste will not be brought into contact with the rear surface of the semiconductor device. Incidentally, like the case of Fig. 1C, the rear surface of the semiconductor device is covered with the insulating resin 62 so that only the areas of the O marks 92 may be exposed.

A third modification is shown in Fig. 1E. In this modification, oppositely to the case of Fig. 1D, convex portions 65 are provided. By adjusting the height of each of the convex portions, even if there is dust on the side of the mounting board, the semiconductor device can be preferably connected to the mounting board. For example, with respect to the semiconductor devices shown in Figs. 1B and 1C, when there is dust between the semiconductor device and the mounting board, solder materials are not be fused with each other, which gives rise to poor soldering. The provision of the convex portions can solve this problem.

Embodiment 2 explaining the semiconductor device according to the invention.

Fig. 2A is a plan view of a semiconductor device according to the invention. Figs. 2B–2E are sectional views taken in line A–A in Fig. 2A. Figs. 2B–2E show the rear-surface structures of the semiconductor device like the first embodiment.

The feature of this embodiment resides in that the semiconductor chips 54, 55 for face-down are adopted so that the external connecting electrodes 52 can be arranged immediately below the semiconductor chip, thereby reducing the planar area and thickness of the semiconductor device.

Each of the first semiconductor chip 54 and the second semiconductor chip 55 may be a bare chip, a flip-chip, SMD, a wafer scale CSP, etc. The external connecting electrodes 52 are formed at the positions corresponding to the electrodes on the semiconductor chips 54, 55. The external connecting electrodes 52 and electrodes of the semiconductor chips 54, 55 are connected to each other by connecting means. This connecting means may be an Au bump, brazing material, soldering ball, conductive ball, anisotropic conductive resin, etc.

The bridge(s) 53 is formed integrally to the external connecting electrodes 52a, 52b. It is extended from the bonding pad 59 of the first semiconductor chip 54 to the bonding pad 60 of the second semiconductor chip 55.

The semiconductor device, in which heat conducts only through the solder ball, exhibits poor heat radiating characteristic. However, by exposing the rear surface of the semiconductor chips 54, 55 from the insulating resin 61, or reducing the thickness of the insulating resin on the rear surface of the semiconductor chips 54, 55, the temperature rise in the semiconductor chips can be prevented. A heat radiating fin may be attached to the rear surface of the semiconductor chips.

Embodiment 3 of the semiconductor device according to the invention.

Fig. 3A is a plan view of a semiconductor device according to the invention. Figs. 3B–3E are sectional views taken in line A–A in Fig. 3A. Figs. 3B–3E show four types of rear-surface structures of the semiconductor device like the above two embodiments.

In this embodiment, the semiconductor chip 55 is superposed on the first semiconductor chip 54. In this embodiment, although two semiconductor chips are stacked, three or more chips may be stacked. Further, since they are connected using metallic wires, they are stacked in such a manner that the upper semiconductor chip is formed to have a smaller size than the lower semiconductor chip, and around the upper semiconductor chip, the bonding pads of the lower semiconductor chip are exposed.

First of all, a die pad 50 is present and the external connecting electrodes 52 are provided around the die pad 50. The front surface of the external connecting electrode serves as a bonding pad, whereas the rear surface thereof is externally connected. The external connecting electrodes 52 include a bridge(s) 52C which connects a first semiconductor chip 54 and a second semiconductor chip 55. The desired number of bridge(s) is formed from the standpoint of the connection of these electrodes.

The first semiconductor chip 54 is fixed onto the die pad 50. The fixing means is selected according to whether the first semiconductor chip 54 is fixed at a prescribed potential or is floating. Specifically, where it is fixed at the prescribed potential, it is fixed using solder or conductive paste. Where it is floating, it is fixed using insulating adhesive. Further, the second semiconductor chip 55 is fixed onto the first semiconductor chip 54 using the insulating adhesive. The bonding pads 58A of the first semiconductor chip 54 are connected to the external connecting electrodes 52A by metallic wires 56A, whereas the bonding pads 58B of the second semiconductor chip 55 are connected to the external connecting electrodes 52B by the metallic wires 56B.

On the other hand, the first semiconductor chip 54 and the second semiconductor chip 55 are connected in such a manner that the bonding pad 59a of the former and the external connecting electrode 52C are connected by a metallic wire 60, whereas the external connecting electrode 52C and the bonding pad 59b of the second semiconductor chip 55 are connected by the metallic wire 60. Incidentally, the external connecting electrode 52C is connected to at least two metallic wires so that its size may be larger than that of the other connecting electrodes.

In this configuration described above in which the external connecting electrode 52C is provided, all the metallic wires on the side of each of the first and second semiconductor chips 54, 55 are made connectable by ball bonding.

As understood from the description of Figs. 7–11, the external connecting electrode 52 are supported in such a manner that the conductive foil is half-etched and they are molded and supported by insulating resin 61 before they are completely separated.

The feature of this invention resides in that the external connecting electrodes 52 are not supported by a coupling piece such as a supporting lead and tab suspending lead,

but are independently sealed by insulating resin 61. In addition, the feature resides in that these independent external connecting electrodes 52 are sealed without using the adhesive tape. Therefore, the completed product of the semiconductor device has no cutting portion of the above coupling piece.

A conventional lead frame has been completed by cutting the coupling member such as a suspending lead and a tie bar. Namely, the lead is machined as a completed product from the front surface to the side and rear surfaces thereof. The lead from which is a completed product requires a coupling member. After the semiconductor chip is mounted on the lead frame, it is sealed by insulating resin, and the coupling member is cut. Thus, the bridge arranged in the form of an island without being connected to anywhere must be fixed by the supporting member such as the adhesive tape.

On the other hand, in accordance with this invention, on the side of a lead frame manufacturer, the conductive foil is half-etched, and the external connecting electrodes 52 are supplied, in a semi-completed state, to a semiconductor manufacturer. On the side of the semiconductor manufacturer, the semiconductor device is subjected to the packaging, electric connection and sealing by insulating resin. Finally, the rear surfaces of the external connecting electrode 52 is treated such as to be divided over the whole surface thereof. Therefore, the semiconductor device can be completed without adopting the coupling member such as the tab suspending lead and adhesive tape, and with no mechanical separation of the coupling member.

Onto the rear surface of the insulating resin 61, the die pad 50 and the external connecting electrodes 52 shown in Fig. 3A are exposed. This is shown in Fig. 3B. The semiconductor device is secured on a mounting board at the electrodes formed on the mounting board to correspond to the above exposed areas. In this case, the heat generated from the semiconductor chip radiated toward the electrodes on the mounting board through the die pad 50 having excellent thermal conductivity. The conventional semiconductor, in which the entire area is packaged or only the solder ball is made of a thermally conductive member in SMD, exhibits poor heat radiating characteristic, and hence could not show the greatest capability of the semiconductor chip. In contrast, the semiconductor device according to this embodiment exhibits excellent heat radiating characteristic and can show

the great capability of the semiconductor chip.

Fig. 3C shows a first modification of the above structure (Fig. 3B). In Fig. 3B, in which the shaded areas are exposed, it was difficult to extend the wirings on the mounting board to the rear surface of the semiconductor device. Further, when a brazing material is applied to the external connecting electrode 52 and die pad 50, the thickness of the solder differs because of a difference in the areas, thus giving rise to poor electrical connection.

This invention intends to solve the above problem by forming an insulating film 62 on the rear surface of the semiconductor device as shown in Fig. 3C. The dotted circles O 92 shown in Fig. 3A show the external connecting electrodes 52 and die pad 50 exposed from the insulating film 62. In other words, since the other areas than the circle O marks 92 are covered with the insulating film 62, the wirings formed on the mounting board can be extended to the rear surface of the semiconductor device. Since the areas of the O marks 92 are approximately equal to one another, the thickness of the brazing material does not substantially differ. This applies after solder printing or reflow, and also applies to the conductive paste such as Ag, Au, Ag-Pd.

A second modification is shown in Fig. 3D. As seen from Fig. 3D, the rear surface of each of the die pads 50 and the external connecting electrodes 52 is formed to be concave from the that of the insulating resin 61. By adjusting the depth of these concave portions 63, the amount of the brazing material and conductive paste formed there can be controlled to adjust the bonding strength. Further, because of the presence of the convex portions 64 of the insulating resin 61, the solder or conductive paste will not be brought into contact with the rear surface of the semiconductor device. Incidentally, like the case of Fig. 3C, the rear surface of the semiconductor device is covered with the insulating resin 62 so that only the areas of the O marks 92 may be exposed.

A third modification is shown in Fig. 3E. In this modification, oppositely to the case of Fig. 3D, convex portions 65 are provided. By adjusting the height of each of the convex portions, even if there is dust on the side of the mounting board, the semiconductor device can be preferably connected to the mounting board. For example, with respect to the semiconductor devices shown in Figs. 3B and 3C, when there is dust between the semiconductor device and the mounting board, solder materials are not be fused with each

other, which gives rise to poor soldering. The provision of the convex portions can solve this problem. This applies to the semiconductor device shown in Fig. 3D.

Embodiment 4 explaining the semiconductor device according to the invention.

This embodiment is shown in Fig. 4. Fig. 4 is a combination of Figs. 1 and 3. On the first die pad 50, the semiconductor chips 70 and 71 are stacked like the structure shown in Fig. 3. Further, on the second die pad 51, a third semiconductor chip 73 is fixed. The first semiconductor chip 70, the second semiconductor chip 71 and the third semiconductor chip 73 are connected to one another through the external connecting electrodes 52 and bridge(s) 53 on the basis of a prescribed electric connection.

The detailed explanation has been made in connection with Figs. 1 and 3 will not be given here.

Embodiment 5 explaining the semiconductor device according to the invention.

This embodiment is shown in Fig. 5. Fig. 5 shows a modification of Fig. 1 in which a circuit element is connected between a bridge 53A and a bridge 53B. Now, the circuit element is a chip capacitor C.

Embodiment 6 explaining the semiconductor device according to the invention

This embodiment is shown in Fig. 6. Fig. 6 shows a modification of Fig. 3 in which a circuit element, e.g. a chip capacitor C is connected between the two connecting electrodes.

Embodiment 7 explaining the method of manufacturing the semiconductor device

Referring to Figs. 7 to 11, an explanation will be given of the method of manufacturing a semiconductor device 80 using a conductive foil mainly made of Cu.

First, as seen from Fig. 7, a plate 81 made of a conductive foil is prepared. The plate 81 has a first surface 82 and second surface 83 which are flat. The second surface 83 is covered with a conductive film 84 or photoresist having a conductive pattern which corresponds to a hatched portion in Fig. 8. Incidentally, where the photoresist is adopted in place of the conductive film, the conductive film is formed below the photoresist at the portion corresponding to the bonding pad.

Next, the plate 81 is half-etched through the conductive film 84 or photoresist. The depth of etching may be shallower than the thickness of the plate 81. Incidentally, it should

be noted that when the depth of etching is shallower, it is possible to form a finer pattern.

By half-etching, conductive patterns are formed in convex shapes on the second surface 83 of the plate 81. The plate 81 may be a laminated body of Cu-Al or Al-Cu-Al. Particularly, the laminated body of Al-Cu-Al can prevent warp resulting from the difference in their thermal expansion coefficient (see Fig. 8 hitherto).

Subsequently, semiconductor elements 85 are fixed onto corresponding areas of the plate. The bonding electrodes of each semiconductor element 85 are electrically connected to first pads 86. In the example as shown, since the semiconductor element 85 is mounted in a face-up form, metallic wired 87 are adopted as a connecting means.

In the above bonding step, since the first pads 86 are integral to the plate 81, and the rear surface of the plate 81 is flat, the plate is brought into contact in plane with a table for a bonding machine. When the plate 81 is completely secured to the bonding table, with no displacement of the first pads 86, bonding energy can be effectively conducted to the metallic wires 87 and first pads 86. Thus, the bonding strength of the metallic wires can be improved. The bonding table can be secured by forming a plurality of vacuum sucking holes on the entire surface of the table.

Where a face-down type of semiconductor element is adopted, the solder balls or bumps of Au or solder are formed for connection of its electrodes. With the electrodes on the semiconductor element 85 arranged immediately below which the corresponding first pads 86 are located, both are fixed to each other (see Fig. 2 as regards the details).

Passive elements may be bonded to the pads 86 through the brazing material such as solder and conductive paste such as Ag paste. The passive elements which can be now adopted are a chip resistor, a chip capacitor, a printed resistor, a coil, etc. (see Fig. 9 hitherto).

A layer of insulating resin 89 is formed to cover the conductive pattern, semiconductor element 85 and connecting means. The insulating resin may be either thermoplastic or thermosetting.

The layer of insulating resin 89 can be formed by the technique of transfer mold, injection mold, dipping or applying. Specifically, the thermosetting resin such as epoxy resin can be formed by the transfer mold, whereas the thermoplastic resin such as

liquid-crystal polymer, polyphenylene sulfide, etc. can be formed by injection mold.

In this embodiment, the thickness of the insulating resin is adjusted so that the thickness of about 100 μm above the top of the metallic wire 87 is covered. This thickness can be increased or decreased in view of the strength of the semiconductor device.

Since the conductive patterns are formed integrally to the sheet-like plate 81, during the implantation, their displacement does not occur unless the displacement of the plate 81 does not occur. The rear surface of the plate 81 can be secured to a lower mold by vacuum sucking.

Thus, the conductive patterns formed as convex portions and semiconductor device are embedded in the insulating resin 89. The portion of the plate 81 lower than the convex portions is exposed on the rear surface (see Fig. 10 hitherto).

Subsequently, the plate 81 exposed to the rear surface of the insulating resin 89 is removed to separate the conductive patterns into individual segments.

The step of separation can be implemented by various techniques. The rear surface of the plate may be removed by etching, or by polishing or griding. Both may be adopted. For example, when the plate is ground until the insulating resin 89 is exposed, the grinding residue of the plate 81 or metal of thin burr extended outwardly will encroach on the insulating resin 89. In order to obviate such inconvenience, cutting-down is stopped immediately before the insulating resin 89 is exposed. Thereafter, the conductive patterns are separated into individual segments by etching. In this case, the metal of the plate 81 does not encroach on the insulating resin between the individual patterns. Thus, short-circuiting between the conductive patterns arranged at minute intervals can be prevented.

Where a plurality of units each constituting a semiconductor device 80 are formed, after the step of separation, a step of dicing the entire resultant body into individual semiconductor devices 80 must be carried out.

In this embodiment, a dicing apparatus was used for the purpose of separation. This separation may be also carried out by chocolate break, pressing or cutting (see Fig. 11 hitherto).

Through the manufacturing process hitherto described, a miniaturized package can

be realized by three components of a plurality of conductive patterns, semiconductor elements 85 and insulating resin 89.

An explanation will be given of the meritorious effects obtained by the manufacturing process described above.

First, since the conductive patterns, which are formed by the half-etching, are supported integrally to the plate, the board which was conventionally used as a supporting board is not required.

Secondly, since the plate can include conductive patterns which have becomes convex as a result of half-etching, the conductive patterns has been miniaturized. Therefore, the width of each conductive pattern and interval between the conductive patterns can be decreased, thereby manufacturing a package with a small planar size.

Thirdly, since the semiconductor device is constituted by the above three components, it can be constituted by a necessary and minimum number of components. Thus, a low-profiled semiconductor device can be manufactured for greatly reduced cost without using unnecessary material.

Fourthly, the die pad, external connecting electrode, bridge and wirings are formed as convex portions by half-etching. Since the separation into the individual chips is carried out after sealing, the tie bar or suspending leads are not necessary. Forming and cutting the tie bar is not required in this invention.

In addition, the bridge can be formed with no support by the adhesive tape.

Fifthly, after the conductive patterns formed as convex portions are embedded in the insulating resin, the plate is removed from the rear surface of the insulating resin to separate the lead into individual lead portions. Therefore, unlike the conventional lead frame, resin burr generated between the leads can be eliminated.

Sixthly, since the rear surface of each of the semiconductor elements is exposed from that of the insulating resin, the heat generated from the semiconductor device according to this invention can be discharged effectively from its rear surface.

As understood from the description hitherto made, this invention has a structure in which the conductive patterns can be formed by half-etching through the conductive film or photoresist. Further, the plate is not stamped out from the front to the rear by pressing

or etching, but its stamping is stopped on the way so that it can be formed into conductive patterns of the external connecting electrodes and bridges. Because of the structure permitting the half-etching to be adopted, the interval between the conductive patterns can be decreased, thereby making more miniaturized patterns. Further, since the die pads, external connecting electrodes and bridges can be formed integrally to the plate, their deformation or warp can be suppressed, thereby making the tie bar and suspending lead unnecessary. Further, after the plate has been completely fixed by sealing the insulating resin, the conductive patterns can be separated by grinding or etching the rear surface of the plate. Thus, the conductive patterns can be arranged at prescribed positions with no displacement. Particularly, although the bridges have been supported by the adhesive tape, this invention permits them to embedded into the insulating resin without adopting such a supporting means.

Since the insulating resin is formed on the sheet-like conductive foil half-etched, burr generated between the leads can be eliminated.

Where the plate is mainly made of Cu and the conductive film is made of Ni, Ag, Au, or Pd, the conductive film can be used as an etching mask. Further, the half-etching permits the side of the plate to be formed into a warping structure or an eave to be formed on the surface of the conductive pattern, thereby giving the anchor effect. Thus, coming-off or warping of the conductive patterns located on the rear surface of the insulating resin can be prevented.

The semiconductor device manufactured from the plate is composed of a necessary and minimum number of components of a semiconductor element, conductive paths such as conductive patterns and insulating resin so that the semiconductor device can be realized with no useless resource. Thus, the semiconductor device can be realized with reduced cost. By adopting the optimum thickness of each of the covering insulating resin and the conductive foil, a greatly miniaturized, low-profiled and light-weight semiconductor device can be realized.

Further, where the semiconductor element is directly fixed to the die pad through the conductive film of brazing material, Au, Ag, etc., the rear surface of the die pad is exposed. Therefore, the heat generated from the semiconductor element can be directly

conducted to the mounting board through the die pad. Particularly, this heat radiating capability permits a power element to be mounted.

The semiconductor device according to this invention has a flat surface on which the rear surface of a separating groove is substantially flush with that of the conductive patterns. Therefore, when a QFP with a small pitch is mounted on the mounting board, the semiconductor device itself can be shifted horizontally as it is. The displacement of the external electrodes can be made very easily.

The semiconductor elements are entirely supported by the entire plate until it is covered with the insulating resin. In the separation of the conductive patterns and their dicing, the insulating resin serves as a supporting board. Therefore, as described in connection with the prior art, the supporting board can be omitted. This reduces the production cost of the semiconductor device.

ABSTRACT OF THE DISCLOSURE

Die pads 50, 51, an external connecting electrode 52 and a bridge are covered with an insulating resin after half-etching, formed into a single package without a coupling member such as a supporting lead or adhesive tape. In addition, since no supporting board is required, a low-profile semiconductor device with improved heat radiation can be provided.